FIG. 1

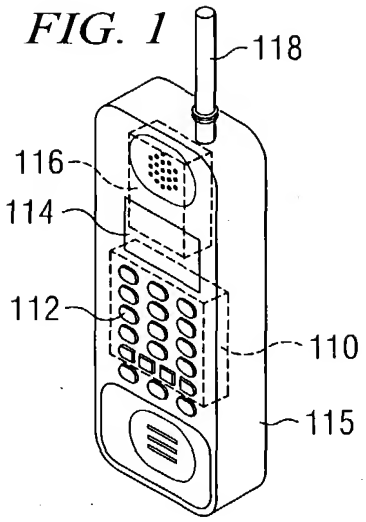


FIG. 4

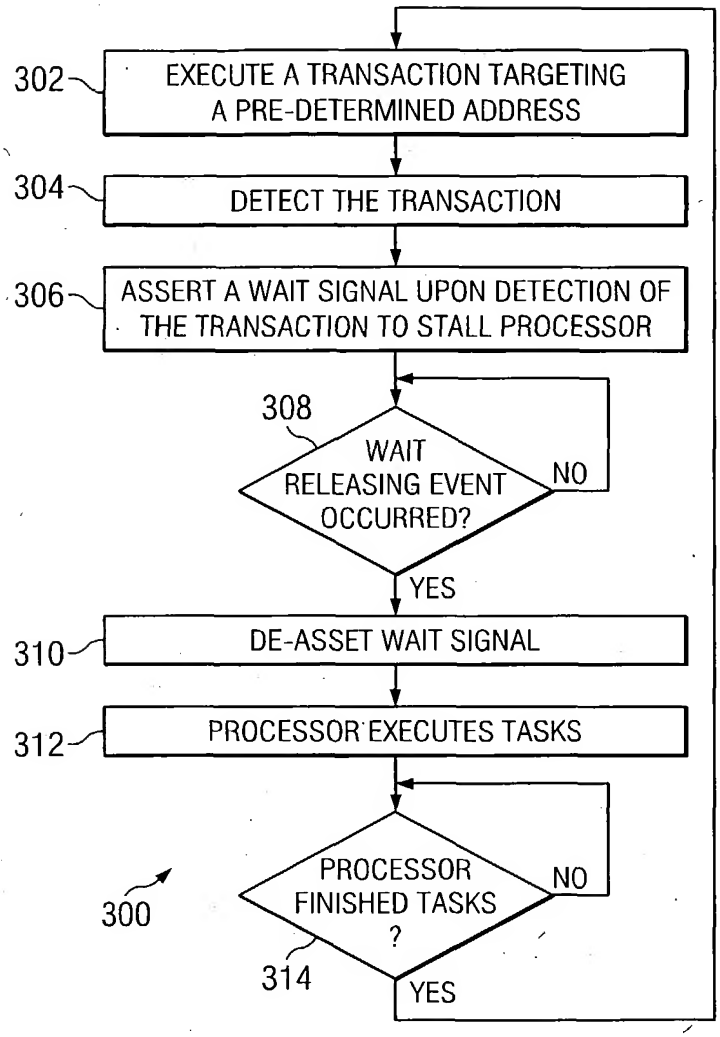


FIG. 2a

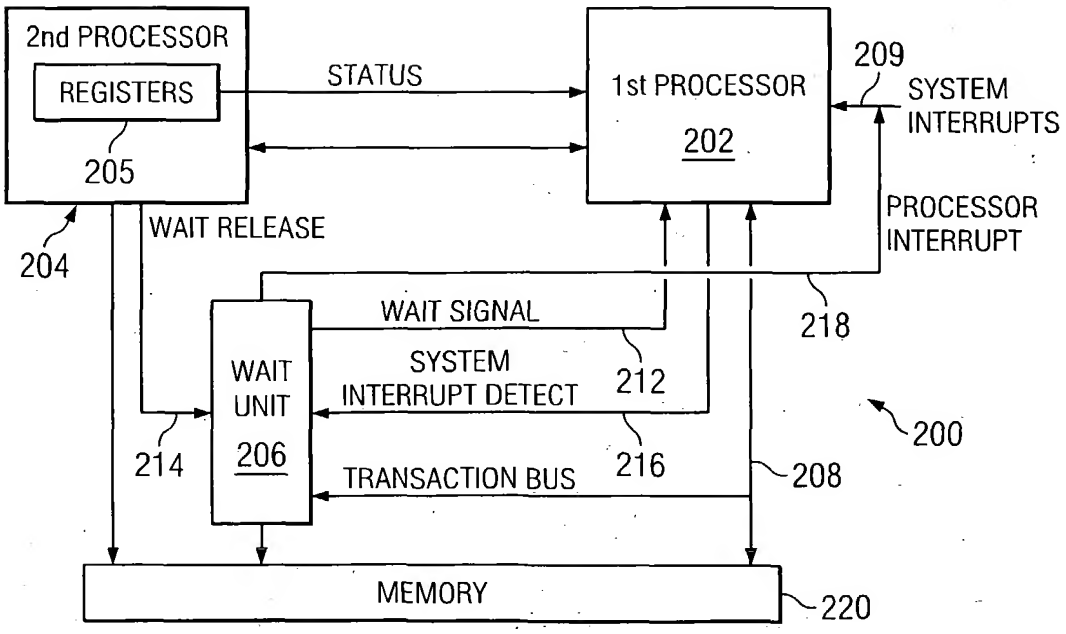


FIG. 2b

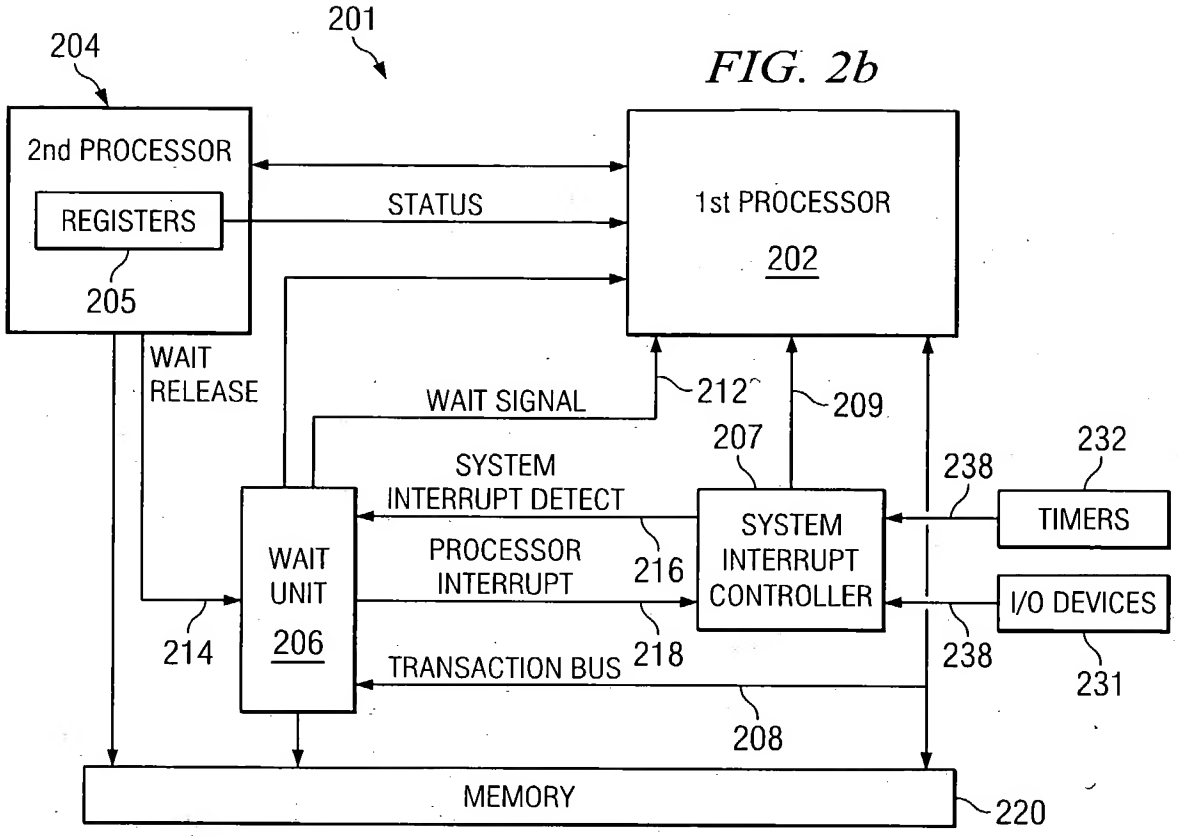
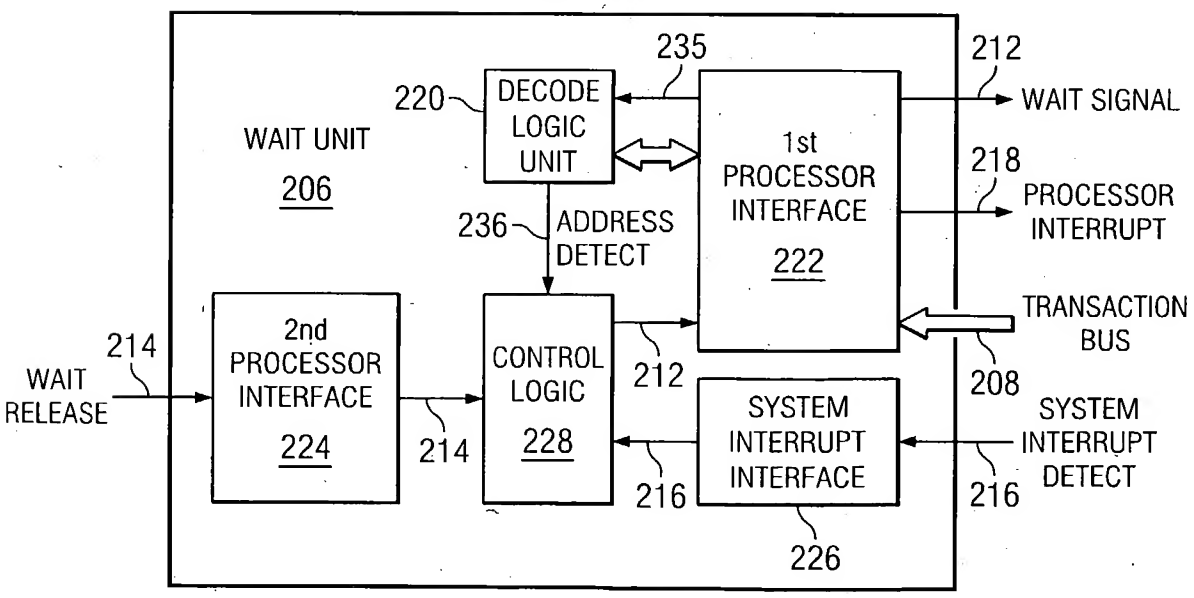

201
204
2nd PROCESSOR
REGISTERS
205
STATUS
1st PROCESSOR
202
WAIT RELEASE
WAIT SIGNAL
212
209
207
232
238
SYSTEM INTERRUPT DETECT
TIMERS
WAIT UNIT
206
PROCESSOR INTERRUPT
216
SYSTEM INTERRUPT CONTROLLER
I/O DEVICES
214
218
238
TRANSACTION BUS
231
208
MEMORY
220

FIG. 3


235
212
220
DECODE LOGIC UNIT
WAIT SIGNAL
WAIT UNIT
206
1st PROCESSOR INTERFACE
222
218
PROCESSOR INTERRUPT
236
ADDRESS DETECT
TRANSACTION BUS
214
2nd PROCESSOR INTERFACE
224
CONTROL LOGIC
228
212
208
WAIT RELEASE
214
SYSTEM INTERRUPT INTERFACE
SYSTEM INTERRUPT DETECT
216
216
226